In the Claims:

Please enter new Claims 59-104 as indicated below. In particular, new claims 59-104 correspond identically to Claims 13-58 which were canceled from the Reissue Application No. 10/071,647 in the Amendment of November 25, 2003. New Claims 59-104 also correspond identically to Claims 13-58 which were allowed in related divisional Reissue Application No. 10/304,440. Claims 1-12 have been maintained as issued in U.S. Patent No. 6,022,753, and Claims 1-12 were indicated allowable in January 31, 2003.

1. (original) A manufacturing method of a thin film transistor (TFT) for a liquid crystal display comprising the steps of:

preparing a transparent substrate having a first and a second surfaces opposite each other;

forming a gate wire including a plurality of gate lines and a gate electrode connected to one of the gate lines, a channel layer located at a position corresponding to the gate electrode, a gate insulating layer between the channel layer and the gate electrode, and a data wire which includes a plurality of data lines defining a pixel region enclosed by the gate lines and the data lines, a source electrode connected to one of the data lines and the channel layer, and a drain electrode connected to the channel layer and separated from the source electrode on the first surface of the substrate;

depositing a passivation layer over the first surface of the substrate;

patterning the passivation layer to form a first contact hole exposing a portion of the drain electrode;

depositing a transparent conductive layer;

coating a negative photoresist on the transparent conductive layer;

front exposing the negative photoresist by irradiating light from the first surface of the substrate using a first mask having first openings at positions corresponding to the first contact hole and the pixel region;

developing the negative photoresist; and

etching the transparent conductive layer by using the negative photoresist as an etch mask to form a pixel electrode connected to the drain electrode via the first contact hole.

2. (original) The manufacturing method of claim 1, wherein the gate wire further includes a plurality of gate pads connected to the respective gate lines and formed outside the pixel regions, and the data wire further includes a plurality of data pads connected to the respective data lines and formed outside the pixel regions,

the method further comprising the step of forming second contact holes and third contact holes exposing the gate pads and the data pads, respectively, and

wherein the first mask has second openings at positions corresponding to the second contact holes and the third contact holes.

3. (original) The manufacturing method of claim 1, further comprising the step of forming a storage wire which includes a storage line parallel to the gate lines and a storage pad connected to the storage line.

4. (original) The manufacturing method of claim 3, further comprising the steps of:

forming a storage electrode overlapping the storage line via the gate insulating layer; and

forming a second contact hole exposing the storage electrode in the passivation layer,

wherein the pixel electrode is connected to the storage electrode through the second contact hole.

5. (original) The manufacturing method of claim 1, further comprising the steps of:

forming a storage electrode overlapping one of the gate lines via the gate insulating layer; and

forming a second contact hole exposing the storage electrode in the passivation layer,

wherein the pixel electrode is connected to the storage electrode through the second contact hole, and the first mask has a second opening at a position corresponding to the second contact hole.

6. (original) A manufacturing method of a thin film transistor (TFT) for a liquid crystal display comprising the steps of:

preparing a transparent substrate a first and a second surfaces opposite each other;

forming a gate wire including a plurality of gate lines and a gate electrode connected to one of the gate lines, a channel layer located at a position corresponding to the gate electrode, a gate insulating layer between the channel layer and the gate electrode, and a data wire which includes a plurality of data lines defining a pixel region enclosed by the gate lines and the data lines, a source electrode connected to one of the data lines and the channel layer, and a drain electrode connected to the channel layer and separated from the source electrode on the first surface of the substrate;

depositing a passivation layer over the first surface of the substrate;

patterning the passivation layer to form a first contact hole exposing a portion of the drain electrode;

depositing a transparent conductive layer;

coating a negative photoresist on the transparent conductive layer;

rear exposing the negative photoresist by irradiating light from the second surface of the substrate;

front exposing the negative photoresist by irradiating light from the first surface of the substrate and using a first mask having a first opening at positions corresponding to the first contact hole;

developing the negative photoresist; and

etching the transparent conductive layer by using the negative photoresist as a etch mask to form a pixel electrode connected to the drain electrode via the first contact hole.

7. (original) The manufacturing method of claim 6, wherein the gate wire further includes a plurality of gate pads connected to the respective gate lines and formed outside the pixel regions, and the data wire further includes a plurality of data pads connected to the respective data lines and formed outside the pixel regions,

the method further comprising the step of forming second contact holes and third contact holes exposing the gate pads and the data pads, respectively, and

wherein portions of the negative photoresist outside the pixel regions are not exposed to light in the rear exposing step, and the first mask has second openings at positions corresponding to the second contact holes and the third contact holes.

8. (original) The manufacturing method of claim 6, wherein the gate wire further includes a plurality of gate pads connected to the respective gate lines and formed outside the pixel regions, and the data wire further includes a plurality of data pads connected to the respective data lines and formed outside the pixel regions,

the method further comprising the steps of:

forming second contact holes and third contact holes exposing the gate pads and the data pads, respectively,

wherein, portions of the negative photoresist outside the pixel regions are exposed to light in the rear exposing step, the first mask has second openings at positions corresponding to the second contact holes and the third contact holes, a first transparent conductive pattern separated from the pixel electrode and placed outside the pixel regions is formed in the etching step, and

removing the negative photoresist;

coating a positive photoresist on the first transparent conductive pattern, the pixel electrode and the passivation layer;

front exposing the positive photoresist by using a second mask having a pattern covering portions of the positive photoresist on the pixel regions, the second contact hole and the third contact hole;

developing the positive photoresist; and

etching the first transparent conductive pattern and the pixel electrode by using the positive photoresist as an etch mask.

9. (original) The manufacturing method of claim 8, wherein the second mask has third openings on the gate lines and the data lines.

10. (original) The manufacturing method of claim 6, further comprising the step of forming a storage wire on the substrate, the storage wire including a storage line parallel to the gate line and a storage pad connected to the storage line and partially overlapping the data line via the gate insulating layer on the substrate,

wherein the first mask has a pattern covering a portion of the storage line overlapping the data line.

11. (original) The manufacturing method of claim 10, further comprising the steps of:

forming a storage electrode overlapping the storage line via the gate insulating layer; and

forming a second contact hole exposing the storage electrode in the passivation layer,

wherein the pixel electrode is connected to the storage electrode through the second contact hole.

12. (original) The manufacturing method of claim 6, further comprising the steps of:

forming a storage electrode overlapping the gate line via the gate insulating layer; and

forming a second contact hole exposing the storage electrode in the passivation layer,

wherein the pixel electrode is connected to the storage electrode through the second contact hole, and the first mask has a second opening at a position corresponding to the second contact hole.

Claims 13-58 (Canceled)

59.(new) A liquid crystal display comprising:

an insulating substrate;

a gate wire and a data wire insulated from each other over the substrate, the gate wire including pluralities of gate lines and gate pads, and the data wire including pluralities of data lines and data pads;

a plurality of thin film transistors, each having a drain electrode and a source electrode electrically connected to the data line;

a passivation layer covering the gate wire, the data wire and the thin film transistors and having first, second and third contact holes which expose the gate pad, the data pad and the drain electrode at least in part, respectively;

a pixel electrode on the passivation film, the pixel electrode connected to the drain electrode through the third contact hole and overlapping at least a part of the data lines adjacent to the pixel electrode;

a first conductor on the passivation film, the first conductor connected to the gate pad through the first contact hole; and

a second conductor on the passivation film, the second conductor connected to the data pad through the second contact hole.

60.(new) The liquid crystal display of claim 59, wherein the pixel electrode overlaps at least a part of the gate lines adjacent to the pixel electrode.

61.(new) The liquid crystal display of claim 60, wherein all edges of the pixel electrode overlap the gate lines or the data lines adjacent to the pixel electrode.

62.(new) The liquid crystal display of claim 59, wherein at least an overlapping portion between the pixel electrode and the gate lines has larger width than other overlapping portions between the pixel electrode and the gate lines or the data lines.

63.(new) The liquid crystal display of claim 59, wherein the first and the second conductors and the pixel electrode comprise the same material.

64.(new) The liquid crystal display of claim 63, wherein the pixel electrode comprises a transparent conducting material.

65.(new) The liquid crystal display of claim 63, wherein the pixel electrode comprises ITO.

66.(new) The liquid crystal display of claim 59, further comprising a storage electrode electrically connected to the pixel electrode, the storage electrode including a layer different from the pixel electrode and serving as a terminal of a storage capacitor.

67.(new) The liquid crystal display of claim 66, further comprising a storage line insulated from the storage electrode and overlapping the storage electrode to form another terminal of the storage capacitor.

68.(new) The liquid crystal display of claim 67, wherein the storage electrode has width smaller than width of the storage line.

69.(new) The liquid crystal display of claim 67, wherein the storage line and the gate lines comprise the same material.

70.(new) The liquid crystal display of claim 59, wherein the storage electrode and the data lines comprise the same material.

71.(new) The liquid crystal display of claim 70, wherein the passivation layer further has a fourth contact hole exposing the storage electrode, and the storage electrode is connected to the pixel electrode through the fourth contact hole.

72.(new) The liquid crystal display of claim 59, wherein the thin film transistor further comprises a gate electrode connected to the gate line, a semiconductor layer insulated from the gate electrode, and a doped semiconductor layer on the semiconductor layer, the doped semiconductor layer being in contact with the source electrode and the drain electrode.

73.(new) The liquid crystal display of claim 72, wherein entire portions of the doped semiconductor layer directly contact the semiconductor layer.

74.(new) The liquid crystal display of claim 72, further comprising a gate insulating layer disposed between the gate wire and the data wire.

75.(new) The liquid crystal display of claim 74, wherein at least a part of the data wire is in direct contact with the gate insulating layer.

76.(new) A liquid crystal display comprising:

an insulating substrate;

pluralities of gate lines and data lines insulated from each other over the substrate;

a plurality of thin film transistors, each having a drain electrode and a source electrode electrically connected to the data line;

a passivation layer covering the gate lines, the data lines and the thin film transistors, the passivation layer having a first contact hole which expose the drain electrode at least in part;

a pixel electrode on the passivation film, the pixel electrode connected to the drain electrode through the first contact hole, overlapping a part of the data lines adjacent to the pixel electrode; and

a first conductor including a layer different from the pixel electrode, electrically connected to the pixel electrode and serving as a terminal of a storage capacitor.

77.(new) The liquid crystal display of claim 76, further comprising a second conductor insulated from the first conductor and overlapping the first conductor to form another terminal of the storage capacitor.

78.(new) The liquid crystal display of claim 77, wherein the first conductor has width smaller than width of the second conductor.

79.(new) The liquid crystal display of claim 77, wherein the second conductor and the gate lines comprise the same material.

80.(new) The liquid crystal display of claim 76, wherein the first conductor and the data lines comprise the same material.

81.(new) The liquid crystal display of claim 80, wherein the passivation layer further has a second contact hole exposing the first conductor, and the first conductor is connected to the pixel electrode through the second contact hole.

82.(new) The liquid crystal display of claim 76, wherein the pixel electrode overlaps at least a part of the gate lines adjacent to the pixel electrode.

83.(new) The liquid crystal display of claim 82, wherein all edges of the pixel electrode overlap the gate lines or the data lines adjacent to the pixel electrode.

84.(new) The liquid crystal display of claim 76, wherein at least an overlapping portion between the pixel electrode and the gate lines has larger width than other overlapping portions between the pixel electrode and the gate lines or the data lines.

85.(new) The liquid crystal display of claim 76, wherein the thin film transistor further comprises a gate electrode connected to the gate line, a semiconductor layer insulated from the gate electrode, and a doped semiconductor layer on the semiconductor layer, the doped semiconductor layer being in contact with the source electrode and the drain electrode.

86.(new) The liquid crystal display of claim 85, wherein entire portions of the doped semiconductor layer directly contact the semiconductor layer.

87.(new) The liquid crystal display of claim 85, further comprising a gate insulating layer disposed between the gate lines and the data lines.

88.(new) The liquid crystal display of claim 87, wherein at least a part of the data lines is in direct contact with the gate insulating layer.

89.(new) A liquid crystal display comprising:

an insulating substrate;

a gate line on the insulating substrate;

a data line on the insulating substrate;

a thin film transistor on the insulating substrate wherein the thin film transistor comprises a pair of source/drains wherein a first of the pair of source/drains is coupled to the data line;

a passivation layer on the gate line, on the data line, and on the thin film transistor so that the gate line, the data line, and the thin film transistor are between the insulating substrate and the passivation layer wherein the passivation layer has a contact hole therein exposing a portion of a second of the pair of source/drains of the thin film transistor; and

a pixel electrode on the passivation layer so that the passivation layer is between the pixel electrode and the insulating substrate wherein the pixel electrode is coupled with the second of the pair of source/drains of the thin film transistor through the contact hole in the passivation layer and wherein the pixel electrode extends onto a portion of the data line so that the portion of the data line is between the pixel electrode extending thereon and the insulating substrate.

90.(new) The liquid crystal display of Claim 89 wherein the thin film transistor comprises a semiconductor layer and wherein the semiconductor layer includes the pair of source/drains, the liquid crystal display further comprising:

a gate insulting layer between the semiconductor layer and the gate line.

91.(new) The liquid crystal display of Claim 90 wherein the pixel electrode extends onto a portion of the gate line without extending across the gate line so that the portion of the gate line is between the pixel electrode extending thereon and the insulating substrate.

92.(new) The liquid crystal display of Claim 90 wherein the gate line and the data line cross, the liquid crystal display further comprising:

an insulating layer between the gate line and the data line at the crossing thereof.

93.(new) The liquid crystal display of Claim 92 wherein the insulating layer between the gate line and the data line and the gate insulating layer each comprise a same material and have a same thickness.

94.(new) The liquid crystal display of Claim 93 wherein the insulating layer between the gate line and the data line and the gate insulating layer comprise a same continuous layer.

95.(new) The liquid crystal display of Claim 89 further comprising:

a storage electrode between the insulating substrate and the passivation layer wherein the passivation layer includes a second contact hole therein exposing a portion of the storage electrode and wherein the pixel electrode is coupled with the storage electrode through the second contact hole.

96.(new) The liquid crystal display of Claim 95 further comprising:

a storage line between the storage electrode and the insulating substrate.

97.(new) The liquid crystal display of Claim 96 further comprising:

an insulating layer between the storage line and the storage electrode.

98.(new) The liquid crystal display of Claim 96 wherein the storage line is parallel to the gate line and wherein the storage line crosses the data line wherein the storage line and the data line are electrically insulated at the crossing thereof.

99.(new) The liquid crystal display of Claim 95 wherein the gate line is between the storage electrode and the insulating substrate.

100.(new) The liquid crystal display of Claim 99 further comprising:

an insulating layer between the gate line and the storage electrode.

101.(new) The liquid crystal display of Claim 89 further comprising:

a second gate line on the insulating substrate wherein the first and second gate lines do not cross; and

a second data line on the insulating substrate wherein the first and second data lines do not cross, wherein the first and second gate lines each cross the first and second data lines, wherein the gate lines and data lines are electrically insulated at the crossings thereof, and wherein each of the first and second gate and data lines is between the passivation layer and the insulating substrate.

102.(new) The liquid crystal display of Claim 101 wherein the pixel electrode extends onto portions of each of the first and second gate and date lines.

103.(new) The liquid crystal display of Claim 101 wherein the pixel electrode extends onto portions of each of the first and second gate and date lines without extending across any of the first and second gate and data lines.

104.(new) The liquid crystal display of Claim 89 where in the pixel electrode does not extend across the data line.